CLAIMS:

1. An anti-fuse transistor formed on a semiconductor material comprising:

a polysilicon gate over a channel region in a substrate, the channel having a preset length;

a diffusion region proximate to one end of the channel region; and,

a variable thickness gate oxide between the polysilicon gate and the substrate, the variable thickness gate oxide having an oxide breakdown zone fusible to form a conductive channel between the polysilicon gate and the channel region, a thicker portion of the variable thickness gate oxide being adjacent to the diffusion region.

2. The anti-fuse transistor of claim 1, wherein the variable thickness gate oxide includes

a thick gate oxide between the substrate and the polysilicon gate, the thick gate oxide extending from the one end of the channel region to a predetermined distance of the preset length, and

a thin gate oxide between the substrate and the polysilicon gate, the thin gate oxide extending from the predetermined distance to a second end of the channel region, the thin gate oxide including the oxide breakdown zone.

3. The anti-fuse transistor of claim 2, further including a floating diffusion region proximate to the thin gate oxide.

4. The anti-fuse transistor of claim 3, wherein the floating diffusion region is adjacent to the thin gate oxide.

5. The anti-fuse transistor of claim 4, wherein the thin gate oxide is identical to at least one low voltage transistor gate oxide formed on the semiconductor material.

6. The anti-fuse transistor of claim 5, wherein the thick gate oxide is identical to at least one high voltage transistor gate oxide formed on the semiconductor material.

7. The anti-fuse transistor of claim 6, wherein the thick gate oxide includes a combination of an intermediate gate oxide and the thin gate oxide.

8. The anti-fuse transistor of claim 3, wherein the floating diffusion area, the second end of the channel region and a gate edge of the polysilicon gate have a common edge defined by at least two line segments being at an angle to each other.

9. The anti-fuse transistor of claim 8, wherein the angle is one of 135 degrees and 90 degrees.

10. The anti-fuse transistor of claim 3, wherein the diffusion region has an LDD implant identical to the LDD implant of one of a low voltage transistor, a high voltage transistor, and a combination of both the low and high voltage transistors.

11. The anti-fuse transistor of claim 1, wherein an edge of the diffusion region and a portion of the polysilicon gate is free of salicidation.

12. An anti-fuse memory array comprising:

a plurality of anti-fuse transistors arranged in rows and columns, each anti-fuse transistor including

a polysilicon gate over a channel region in a substrate, the channel having a preset length;

a diffusion region proximate to one end of the channel region;

a variable thickness gate oxide between the polysilicon gate and the substrate, the variable thickness gate oxide having an oxide breakdown zone fusible to form a conductive channel between the polysilicon gate and the channel region, a thicker portion of the variable thickness gate oxide being adjacent to the diffusion region;

bitlines coupled to the diffusion regions of a column of anti-fuse transistors; and,

wordlines coupled to the polysilicon gates of a row of anti-fuse transistors.

13. The anti-fuse memory array of claim 12, wherein the variable thickness gate oxide includes

a thick gate oxide between the substrate and the polysilicon gate, the thick gate oxide extending from the one end of the channel region to a predetermined distance of the preset length, and

a thin gate oxide between the substrate and the polysilicon gate, the thin gate oxide extending from the predetermined distance to a second end of the channel region, the thin gate oxide including the oxide breakdown zone.

14. The anti-fuse memory array of claim 13, further including a sense amplifier coupled to a pair of bitlines through isolation devices.

15. The anti-fuse memory array of claim 14, further including wordline decoding circuitry for selectively accessing one anti-fuse transistor coupled to one of the pair of bitlines for a single-ended sensing operation, and for selectively accessing another anti-fuse transistor coupled to the other of the pair of bitlines for a different address.

16. The anti-fuse memory array of claim 14, further including wordline decoding circuitry for selectively accessing one anti-fuse transistor coupled to one of the pair of bitlines and one anti-fuse transistor coupled to the other of the pair of bitlines for a dual-ended sensing operation.

17. The anti-fuse memory array of claim 13, wherein the column select pass gates have a gate oxide that is the same as the thick gate oxide.

18. A method of forming a variable thickness gate oxide for an anti-fuse transistor, comprising the steps of:

a) growing an intermediate oxide in a channel region of the anti-fuse transistor;

b) removing the intermediate oxide from a thin oxide region of the channel region; and,

c) growing a thin oxide over the thin oxide region and the intermediate oxide in the channel region.

19. The method of claim 18, further including the step of forming a common gate over the thin and intermediate oxide regions

20. The method of claim 18, further including the step of forming a diffusion region adjacent the intermediate oxide.

21. The method of claim 18, further including the step of forming a floating diffusion region adjacent the thin oxide region.

22. The method of claim 19, further including the steps of
selectively growing a salicidation protect oxide over the diffusion region; and,
saliciding a portion of the polysilicon gate and the floating diffusion region.

23. An anti-fuse transistor formed on a semiconductor material comprising:
an active area;
a polysilicon gate formed over the active area to define a fusible edge and an access edge;
a thick gate oxide adjacent to the access edge;
a diffusion region adjacent to the access edge; and
a thin gate oxide adjacent to the fusible edge, the thin gate oxide having a lower breakdown voltage than the thick gate oxide for forming a conductive channel between the polysilicon gate and the diffusion region.

24. The anti-fuse transistor of claim 23, wherein the fusible edge is longer than the access edge.

25. The anti-fuse transistor of claim 24, wherein a length of the fusible edge is defined by at least two line segments of the polysilicon gate being at an angle to each other.

26. The anti-fuse transistor of claim 24, wherein a length of the fusible edge is defined by a width of the active area.

27. The anti-fuse transistor of claim 23, wherein the polysilicon gate defines a channel region between the fusible edge and the access edge, and the thick gate oxide and the thin gate oxide are disposed between the channel region and the polysilicon gate.

28. The anti-fuse transistor of claim 27, wherein the thick gate oxide extends from the access edge to a predetermined length of the channel region, and the thin gate oxide extends from the predetermined length of the channel region to the fusible edge.

29. The anti-fuse transistor of claim 28, wherein the thick gate oxide is a combination of an intermediate oxide and the thin oxide.

30. The anti-fuse transistor of claim 23, wherein the thin gate oxide is identical to a low voltage transistor gate oxide formed on the semiconductor material.

31. The anti-fuse transistor of claim 23, wherein the thick gate oxide is identical to a high voltage transistor gate oxide formed on the semiconductor material.

32. The anti-fuse transistor of claim 23, wherein the polysilicon gate defines a channel region between the fusible edge and the access edge, and the thick gate oxide and the thin gate oxide are disposed between the channel region and the polysilicon gate.

33. The anti-fuse transistor of claim 23, further including a floating diffusion region adjacent the fusible edge.

34. The anti-fuse transistor of claim 33, wherein the polysilicon gate has

a first portion disposed over the thick gate oxide and located adjacent to the diffusion region for defining a channel region, the access edge being defined by a first portion edge, and

a second portion disposed over the thin gate oxide and coupled to the first portion, the fusible edge being defined by a second portion edge, the floating diffusion region being disposed between the fusible edge and the channel region.

35. The anti-fuse transistor of claim 23, wherein a portion of the polysilicon gate and an edge of the diffusion region is free of salicidation.

AMENDED CLAIMS

received by the International Bureau on 10 October 2005 (10.10.05): original claims 1-35 have been replaced by amended claims 1-29 + statement.

What is claimed is:

1. An anti-fuse transistor formed on a semiconductor material comprising:

a polysilicon gate over a channel region in a substrate, the channel having a preset length;

a diffusion region proximate to a first end of the channel region;

an isolation region proximate to a second end of the channel region;

a variable thickness gate oxide between the polysilicon gate and the substrate, the variable thickness gate oxide having

a thick gate oxide portion extending from the first end of the channel region to a predetermined distance of the preset length,

a thin gate oxide portion extending from the predetermined distance to the second end of the channel region;

a breakdown resistant access edge proximate to the first end of the channel region for conducting current between the polysilicon gate and the diffusion region; and

an oxide breakdown zone proximate to the second end of the channel region, the oxide breakdown zone fusible to form a conductive link between the polysilicon gate and the channel region.

2. The anti-fuse transistor of claim 1 wherein the isolation region includes one of a field oxide region, a floating diffusion region and a combination of the field oxide and the floating diffusion regions proximate to the thin gate oxide.

3. The anti-fuse transistor of claim 1, wherein the thin gate oxide portion is identical to at least one low voltage transistor gate oxide formed on the semiconductor material.

4. The anti-fuse transistor of claim 3, wherein the thick gate oxide portion is identical to at least one high voltage transistor gate oxide formed on the semiconductor material.

5. The anti-fuse transistor of claim 4, wherein the thick gate oxide portion includes a combination of an intermediate gate oxide and the thin gate oxide portion.

6. The anti-fuse transistor of claim 2, wherein the floating diffusion region, the second end of the channel region and a gate edge of the polysilicon gate have a common edge defined by at least two line segments being at an angle to each other.

7. The anti-fuse transistor of claim 6, wherein the angle is one of 135 degrees and 90 degrees.

8. The anti-fuse transistor of claim 4, wherein the diffusion region has an LDD implant identical to the LDD implant of one of the low voltage transistor, the high voltage transistor, and a combination of both the low and the high voltage transistors.

9. The anti-fuse transistor of claim 1, wherein an edge of the diffusion region and a portion of the polysilicon gate is free of salicidation.

10. An anti-fuse memory array comprising:

a plurality of anti-fuse transistors arranged in rows and columns, each anti-fuse transistor including

a polysilicon gate over a channel region in a substrate, the channel having a preset length;

a diffusion region proximate to a first end of the channel region;

a variable thickness gate oxide between the polysilicon gate and the substrate, the variable thickness gate oxide having a thick gate oxide portion extending from the first end of the channel region to a predetermined distance of the preset length, and a thin gate oxide portion extending from the predetermined distance to a second end of the channel region,

an oxide breakdown zone proximate to the second end of the channel region fusible to form a conductive link between the polysilicon gate and the channel region;

bitlines coupled to the diffusion regions of a column of anti-fuse transistors; and,

wordlines coupled to the polysilicon gates of a row of anti-fuse transistors.

11. The anti-fuse memory array of claim 10, further including a sense amplifier coupled to a pair of bitlines through isolation devices.

12. The anti-fuse memory array of claim 11, further including wordline decoding circuitry for selectively accessing one anti-fuse transistor coupled to one of the pair of bitlines for a single-ended sensing operation, and for selectively accessing another anti-fuse transistor coupled to the other of the pair of bitlines for a different address.

13. The anti-fuse memory array of claim 11, further including wordline decoding circuitry for selectively accessing one anti-fuse transistor coupled to one of the pair of bitlines and one anti-fuse transistor coupled to the other of the pair of bitlines for a dual-ended sensing operation.

14. The anti-fuse memory array of claim 10, further including column select pass gates coupled to the bitlines, at least one of the column select pass gates having a gate oxide identical to the thick gate oxide portion.

15. A method of forming a variable thickness gate oxide for an anti-fuse transistor having a channel region and a diffusion region, comprising the steps of:

a) forming a field oxide surrounding the channel region and the diffusion region;

b) growing an intermediate oxide in the channel region;

c) removing the intermediate oxide from a thin oxide region of the channel region;

d) growing a thin oxide over the thin oxide region and the intermediate oxide;

e) forming a common gate over the thin oxide, the intermediate oxide and the field oxide; and,

f) forming the diffusion region adjacent the intermediate oxide.

16. The method of claim 15, wherein the anti-fuse transistor and one low voltage transistor are formed on a semiconductor material, the low voltage transistor having a dielectric structure being the same as the thin oxide.

17. The method of claim 15, wherein the step of forming the diffusion region includes simultaneously forming a floating diffusion region adjacent the thin oxide region.

18. The method of claim 15, wherein the intermediate oxide extends from a first edge of the common gate to a predetermined length of the channel region, and the thin gate oxide over the thin oxide region extends from the predetermined length of the channel region to a second edge of the common gate.

19. The method of claim 18, wherein said predetermined length is defined through a masking step.

20. The anti-fuse transistor of claim 15, wherein the thin oxide is formed with the same process steps as for forming a low voltage transistor gate oxide on the same semiconductor material.

21. The anti-fuse transistor of claim 15, wherein a thick oxide consisting of the thin oxide and the intermediate oxide is formed with the same process steps as for forming a high voltage transistor gate oxide on the same semiconductor material.

22. The method of claim 15, further including the steps of

selectively growing a salicidation protect oxide over the diffusion region; and,

saliciding a portion of the common gate and the diffusion region.

23. An anti-fuse transistor formed on a semiconductor material comprising:

an active channel area;

a polysilicon gate formed over the active channel area to define a fusible edge and an access edge;

a thick gate oxide adjacent to the access edge;

a first diffusion region adjacent to the access edge;

a second diffusion region adjacent to the fusible edge; and

a thin gate oxide over the active channel area adjacent to the fusible edge, the thin gate oxide having a lower breakdown voltage than the thick gate oxide for forming a conductive link between the polysilicon gate and the active channel area.

24. The anti-fuse transistor of claim 23, wherein a length of the fusible edge is defined by at least two line segments of the polysilicon gate being at an angle to each other.

25. The anti-fuse transistor of claim 23, wherein a length of the fusible edge is greater than a width of the active channel area.

26. The anti-fuse transistor of claim 23, wherein the polysilicon gate defines the active channel area between the fusible edge and the access edge, and the thick gate oxide and the thin gate oxide are disposed between the channel region and the polysilicon gate, the thick gate oxide extending from the access edge to a predetermined length of the active channel area, and the thin gate oxide extending from the predetermined length of the active channel area to the fusible edge.

27. The anti-fuse transistor of claim 26, wherein the thick gate oxide is a combination of an intermediate oxide and the thin oxide.

28. The anti-fuse transistor of claim 23, wherein the polysilicon gate has

a first portion disposed over the thick gate oxide and located adjacent to the diffusion region for defining the active channel area, the access edge being defined by a first portion edge, and

a second portion disposed over the thin gate oxide and coupled to the first portion, the fusible edge being defined by a second portion edge, the second diffusion region being disposed between the fusible edge and the active channel area.

29. An anti-fuse transistor formed on a semiconductor material comprising:

an active channel area;

a polysilicon gate formed over the active channel area to define a fusible area, an access edge and an isolation edge;

a thick gate oxide adjacent to the access edge;

a diffusion region adjacent to the access edge;

a field oxide adjacent to the isolation edge; and

a thin gate oxide having a fusible area between the thick gate oxide and the isolation edge, the fusible area having a lower breakdown voltage than the thick gate oxide for forming a conductive link between the polysilicon gate and the active channel area.

STATEMENT UNDER ARTICLE 19(1) (RULE 46.4)

The claims have been amended to clarify the claimed invention in response to the Written Opinion of the International Searching Authority mailed August 10, 2005. In particular, the claims have been amended to distinguish the claimed invention from cited references D1, D2 and D3.